

What is claimed is:

1. An integrated circuit comprising:  
a semiconductor substrate;  
5 a buried insulation layer over the semiconductor substrate;  
a semiconductor mesa over the buried insulation layer; and,  
a guard ring substantially surrounding the  
10 semiconductor mesa, wherein the guard ring is in contact with the semiconductor substrate, and wherein the guard ring is arranged to provide RF isolation for the semiconductor mesa.
- 15 2. The integrated circuit of claim 1 wherein the semiconductor substrate comprises a high resistivity semiconductor substrate.
- 20 3. The integrated circuit of claim 1 wherein the semiconductor substrate comprises a silicon substrate, wherein the buried insulating layer comprises a buried silicon oxide layer, and wherein the semiconductor mesa comprises a silicon mesa.

4. The integrated circuit of claim 3 wherein the silicon substrate comprises a high resistivity silicon substrate.

5 5. The integrated circuit of claim 1 wherein the semiconductor substrate is doped in an area that is contacted by the guard ring.

6. The integrated circuit of claim 5 wherein  
10 the semiconductor substrate comprises a high resistivity semiconductor substrate.

7. The integrated circuit of claim 5 wherein the semiconductor substrate comprises a silicon  
15 substrate, wherein the buried insulating layer comprises a buried silicon oxide layer, and wherein the semiconductor mesa comprises a silicon mesa.

8. The integrated circuit of claim 7 wherein  
20 the silicon substrate comprises a high resistivity silicon substrate.

9. The integrated circuit of claim 1 further comprising an insulating ring between the guard ring and the semiconductor mesa, wherein the insulating ring surrounds the semiconductor mesa.

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10. The integrated circuit of claim 9 wherein the semiconductor substrate comprises a high resistivity semiconductor substrate.

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11. The integrated circuit of claim 9 wherein the semiconductor substrate comprises a silicon substrate, wherein the buried insulating layer comprises a buried silicon oxide layer, wherein the insulating ring comprises a silicon oxide insulating ring, and wherein  
15 the semiconductor mesa comprises a silicon mesa.

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12. The integrated circuit of claim 11 wherein the silicon substrate comprises a high resistivity silicon substrate.

13. The integrated circuit of claim 9 wherein the semiconductor substrate is doped in an area that is contacted by the guard ring.

14. The integrated circuit of claim 13 wherein the semiconductor substrate comprises a high resistivity semiconductor substrate.

5           15. The integrated circuit of claim 13 wherein the semiconductor substrate comprises a silicon substrate, wherein the buried insulating layer comprises a buried silicon oxide layer, wherein the insulating ring comprises a silicon oxide insulating ring, and wherein  
10 the semiconductor mesa comprises a silicon mesa.

16. The integrated circuit of claim 15 wherein the silicon substrate comprises a high resistivity silicon substrate.

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17. The integrated circuit of claim 1 wherein the guard ring comprises a low resistivity guard ring.

18. The integrated circuit of claim 1 wherein  
20 the guard ring comprises a metal guard ring.

19. The integrated circuit of claim 18 wherein the metal guard ring comprises a tungsten guard ring.

20. An integrated circuit comprising:
- a semiconductor substrate;
  - a buried insulation layer over the semiconductor substrate;
  - 5 a first semiconductor mesa over the buried insulation layer;
  - a second semiconductor mesa over the buried insulation layer;
  - a first guard ring substantially surrounding
  - 10 the first semiconductor mesa, wherein the first guard ring is in contact with the semiconductor substrate, and wherein the first guard ring is arranged to provide RF isolation for the first semiconductor mesa; and,
  - a second guard ring substantially surrounding
  - 15 the second semiconductor mesa, wherein the second guard ring is in contact with the semiconductor substrate, and wherein the second guard ring is arranged to provide RF isolation for the second semiconductor mesa.
- 20 21. The integrated circuit of claim 20 further comprising a third guard ring between the first and second guard rings, wherein the third guard ring is in contact with the semiconductor substrate, and wherein the

third guard ring is arranged to provided further RF  
isolation for the first and second semiconductor mesas.

22. The integrated circuit of claim 21 wherein  
5 the semiconductor substrate comprises a high resistivity  
semiconductor substrate.

23. The integrated circuit of claim 21 wherein  
the semiconductor substrate comprises a silicon  
10 substrate, wherein the buried insulating layer comprises  
a buried silicon oxide layer, wherein the first  
semiconductor mesa comprises a first silicon mesa, and  
wherein the second semiconductor mesa comprises a second  
silicon mesa.

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24. The integrated circuit of claim 21 wherein  
the semiconductor substrate is doped in a first area that  
is contacted by the first metal guard ring, wherein the  
semiconductor substrate is doped in a second area that is  
20 contacted by the second metal guard ring, and wherein the  
semiconductor substrate is doped in a third area that is  
contacted by the third metal guard ring.

25. The integrated circuit of claim 21 further comprising first and second insulating rings, wherein the first insulating ring surrounds the first semiconductor mesa and is between the first metal guard ring and the first semiconductor mesa, and wherein the second insulating ring surrounds the second semiconductor mesa and is between the second metal guard ring and the second semiconductor mesa.

26. The integrated circuit of claim 25 wherein the semiconductor substrate is doped in a first area that is contacted by the first metal guard ring, and wherein the semiconductor substrate is doped in a second area that is contacted by the second metal guard ring.

27. The integrated circuit of claim 21 wherein the first guard ring comprises a first low resistivity guard ring, wherein the second guard ring comprises a first low resistivity guard ring, and wherein the third guard ring comprises a third low resistivity guard ring.

28. The integrated circuit of claim 21 wherein  
the first guard ring comprises a first metal guard ring,  
wherein the second guard ring comprises a second metal  
guard ring, and wherein the third guard ring comprises a  
5 third metal guard ring.

29. The integrated circuit of claim 28 wherein  
the first metal guard ring comprises a first tungsten  
guard ring, wherein the second metal guard ring comprises  
10 a second tungsten guard ring, and wherein the third metal  
guard ring comprises a third tungsten guard ring.

30. The integrated circuit of claim 21 wherein  
the first semiconductor mesa is part of a sub-circuit,  
15 wherein the sub-circuit includes one or more other  
semiconductor mesas, wherein the first semiconductor mesa  
and the one or more other semiconductor mesas are  
individually surrounded by the first guard ring, and  
wherein the third guard ring surrounds the first guard  
20 ring.



31. The integrated circuit of claim 20 wherein the semiconductor substrate is doped in a first area that is contacted by the first guard ring, and wherein the semiconductor substrate is doped in a second area that is  
5 contacted by the second guard ring.

32. A method of RF isolating a semiconductor feature of an integrated circuit comprising:  
forming a buried insulation layer over a  
10 semiconductor substrate;  
forming a semiconductor feature in one or more semiconductor layers so that the semiconductor feature is formed over a portion of the buried insulation layer, wherein the buried insulating layer has a trench  
15 therethrough down to the semiconductor substrate that substantially encloses the portion of the buried insulation layer, wherein the one or more semiconductor layers has a trench therethrough that substantially encloses the semiconductor feature, and wherein the  
20 trench through the one or more semiconductor layers substantially aligns with the trench through the buried insulating layer; and,  
filling the trench through the one or more semiconductor layers and the trench through the buried

insulating layer with conducting material having low resistivity so that a conductive guard ring substantially surrounds the semiconductor feature.

5           33. The method of claim 32 wherein the semiconductor substrate comprises a high resistivity semiconductor substrate.

          34. The method of claim 32 further comprising  
10   doping an area of the semiconductor substrate that is contacted by the conductive guard ring.

          35. The method of claim 32 further comprising forming an insulating ring surrounding the semiconductor  
15   feature such that the insulating ring is between the conductive guard ring and the semiconductor feature.

          36. The method of claim 32 wherein the semiconductor feature comprises a first semiconductor  
20   feature, wherein the portion of the buried insulation layer comprises a first portion of the buried insulation layer, wherein the trench through the buried insulating layer comprises a first trench through the buried insulating layer, wherein the trench through the one or

more semiconductor layers comprises a first trench through the one or more semiconductor layers, and wherein the conductive guard ring comprises a first conductive guard ring, the method further comprising:

5           forming a second semiconductor feature in the one or more semiconductor layers so that the second semiconductor feature is formed over a second portion of the buried insulation layer, wherein the buried insulating layer has a second trench therethrough down to  
10 the semiconductor substrate that substantially encloses the second portion of the buried insulation layer, wherein the one or more semiconductor layers has a second trench therethrough that substantially encloses the second semiconductor feature, and wherein the second  
15 trench through the one or more semiconductor layers is substantially aligned with the second trench through the buried insulating layer; and,

          filling the second trench through the one or more semiconductor layers and the second trench through  
20 the buried insulating layer with conducting material having low resistivity so that a second conductive guard ring substantially surrounds the second semiconductor feature.

37. The method of claim 36 further comprising forming a third conductive guard ring between the first and second conductive guard rings, the third conductive guard ring being in contact with the semiconductor substrate.

38. The method of claim 32 further comprising grounding the conductive guard ring.

39. An integrated circuit comprising:  
a semiconductor substrate, the semiconductor substrate forming a first semiconductor layer;  
a semiconductor feature formed in a second semiconductor layer, wherein the second semiconductor layer is over the first semiconductor layer; and,  
a guard ring substantially surrounding the semiconductor feature, wherein the guard ring is in contact with the semiconductor substrate, and wherein the guard ring is arranged to provide RF isolation for the semiconductor feature.